CHAPTER – 7

THE ENHANCEMENT-TYPE MOSFET

There is another class of field-effect transistors that can operate like any other field-effect transistor as long as it is properly biased. It is fabricated like a depletion-type metal-oxide-semiconductor field-effect transistor but without a channel as described in the following paragraphs. The channel is, in fact, created when the transistor is properly biased. Once the channel is created, it can either be an n-channel or a p-channel. We will refer to such a device **as the Metal-Oxide-Semiconductor Field-Effect Transistor or simply the MOSFET**. The n-channel MOSFET is usually referred to as **NMOS** and the p-channel MOSFET as **PMOS**. Let us first understand the construction of an n-channel MOSFET or NMOS.

7.1 Fabrication of an NMOS

The fabrication of an n-channel MOSFET begins with a base (usually called the substrate) that is highly resistive p-type semiconductor. The base forms the body of the transistor. Diffused into the body are two low-resistivity n-type regions that are separated by the p-type substrate as shown in **Figure 7.1**. Just like any other FET, one of the two n-type regions is called the drain and the other is the source.

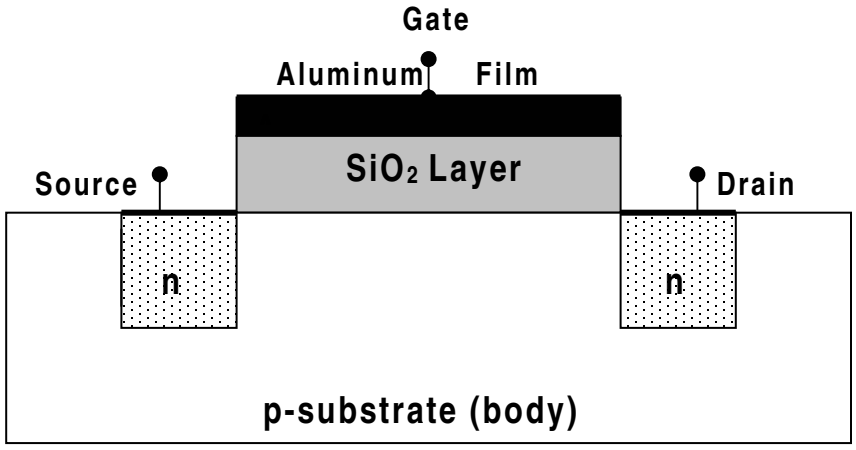


Figure 7.1: Structure of an NMOS

In order to form a gate terminal for the NMOS, a thin layer of silicon dioxide is grown over the surface of the p-type substrate. A thin film of aluminum is deposited over the insulating layer of silicon dioxide. The aluminum film then acts as the gate terminal as shown. By now you must have realized the absence of the n-channel. It is not created as part of the device. As the p-substrate separates the two n-type regions, there is a very high resistance between the drain and the source. Unless the transistor is properly biased, the device is in its cut-off mode**. For this reason, it is a normally OFF device**. On the other hand, the JFET and the DFET are both normally ON devices due to the presence of the channel between the drain and the source terminals.

The thin SiO_2 insulating layer is about 1500 Å. The total chip area required for the fabrication of a FET is less than 5 square mils (1 mil = one-thousandth of an inch). Just for the comparison purposes, about 10 times more chip area is need to manufacture a BJT. This is the main reason for the widespread use of FETs in the fabrication of integrated circuits (ICs).

7.2 Operation of an NMOS

In the fabrication of an NMOS transistor, the gate is insulated from the channel. Therefore, the gate current is negligible regardless of the gate voltage with respect to the source. For this reason, the NMOS is also referred to as an **Insulated Gate Field-Effect Transistor (IGFET).**

Let us first imagine that the drain and the source terminals are held at a common potential as shown in **Figure 7.2**. As the gate terminal is insulated from the channel by the silicon dioxide layer, let us apply a positive voltage at the gate with respect to the source. The application of the positive voltage at the gate with respect to the source (V_{GS}) pulls electrons into the region between the drain and the source. This is due to the capacitor formed by the insulating SiO_2 layer between the gate and the p-type substrate. As V_{GS} is increased, more and more electrons are attracted toward the gate. These negative charges

redistribute themselves in the region between the drain and the source in the form of a thin layer. This layer of free electrons is called an **n-type inversion layer**. As soon as V_{GS} reaches the **threshold voltage** (V_T), the entire region between the drain and the source gets filled with electrons. Thus, a channel has been induced in the p-region just below the gate. The channel now connects the drain to the source. The formation of the channel increases the conductivity of the region between the drain and the source increases which, in turn, allows the current to flow from the drain toward the source when drain is held at a higher potential than the source. Any further increase in V_{GS} widens the channel and further increases its conductivity. This, in turn, increases the drain current. The drain current continues to increase with the increase in the **gate-to-source** voltage. Since the positive gate voltage increases (enhances) the channel's conductivity**, the NMOS is said to operate in its enhancement mode when the gate is positive with respect to the source.**

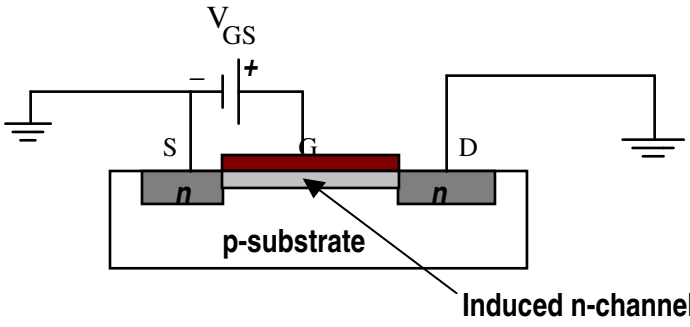


Figure 7.2 Induced n-channel in an NMOS

Let us now apply a positive voltage at the drain with respect to the source (V_{DS}) as shown in **Figure 7.3** while the gate is at a voltage V_{GS} greater than V_T. As soon as V_{DS} becomes greater than zero, there is a current (I_D) from the drain toward the source through the highly conductive channel. However, with the increase in V_{DS}, the gate-to-drain voltage decreases which, in turn, decreases channel's width near the drain terminal. The channel's width near the

source terminal remains the same as long as V_{GS} is held constant. The decrease in channel's width near the drain causes a decrease in its conductivity and an increase in its resistance. As long as the channel exists between the drain and the source, the drain current increases with the increase in the drain-to-source voltage**. This is the linear (or triode) region of operation of the NMOS.**

As we continue to increase V_{DS}, the channel's width near the drain continues to diminish until it pinches off as shown in **Figure 7.3**. This process is commonly referred to as **channel modulation**. At the pinch-off point, the drain-to-source voltage is referred to as the drain-to-source pinch-off voltage V_{DSP}. The channel's width near the drain is almost zero and the channels resistance becomes very high (almost infinite). Any further increase in the drain-to-source voltage does not result in any appreciable increase in the drain current. The device has entered the **saturation region**. In the saturation region, $V_{DS} \geq V_{DSP}$.

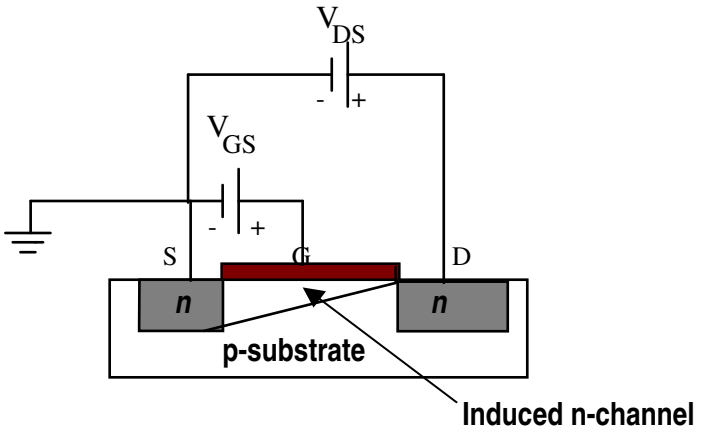


Figure 7.3 Channel modulation of an NMOS

As V_{DS} is increased beyond V_{DSP}, the drain current remains almost constant but the channel modulation continues and the pinch-off point moves toward the source as illustrated in **Figure 7.4**. The transistor continues to operate in the saturation region as long as V_{DS} is less than the breakdown voltage of the device (BV_{DSS}).

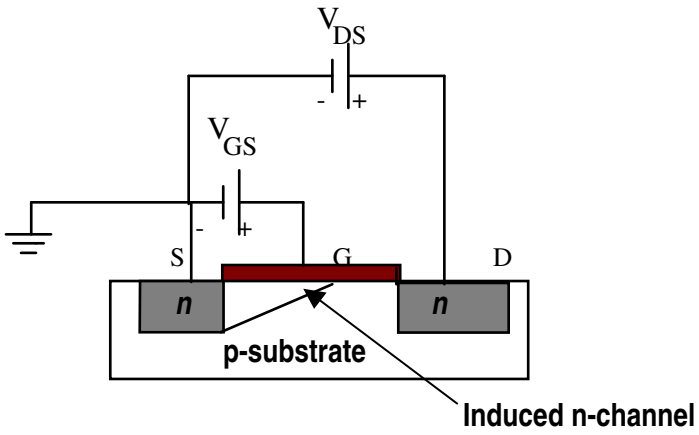


Figure 7.4 Movement of pinch-off point as a function of V_{DS}

For **NDS9410**, an N-channel Enhancement Mode Field-Effect Transistor, the minimum breakdown voltage is 30 V. It can deliver a continuous drain current of 7A and can dissipate maximum power of 2.5 W at a temperature of 25°C. Its gate-to-source threshold voltage has a typical value of 1.4 V but can vary from 1 to 3 V.

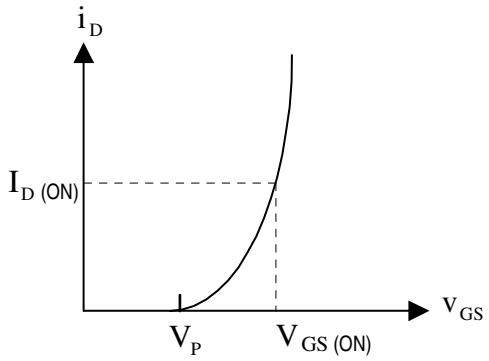


Figure 7.5: Transfer characteristic of an NMOS

7.3 Various Characteristics of an NMOS

The **transfer characteristic** of an n-channel DFET is given in **Figure 7.5** where its threshold voltage is V_T. The data sheet usually provides information on the threshold voltage and another point on the curve as shown. For example, for NDS9410, $I_{D(ON)}$ is 7.7 A when $V_{GS(ON)}$ is 2.7 V and V_{DS} is 2.7 V. Note that the typical value for the threshold voltage V_T for this transistor is 1.4 V.

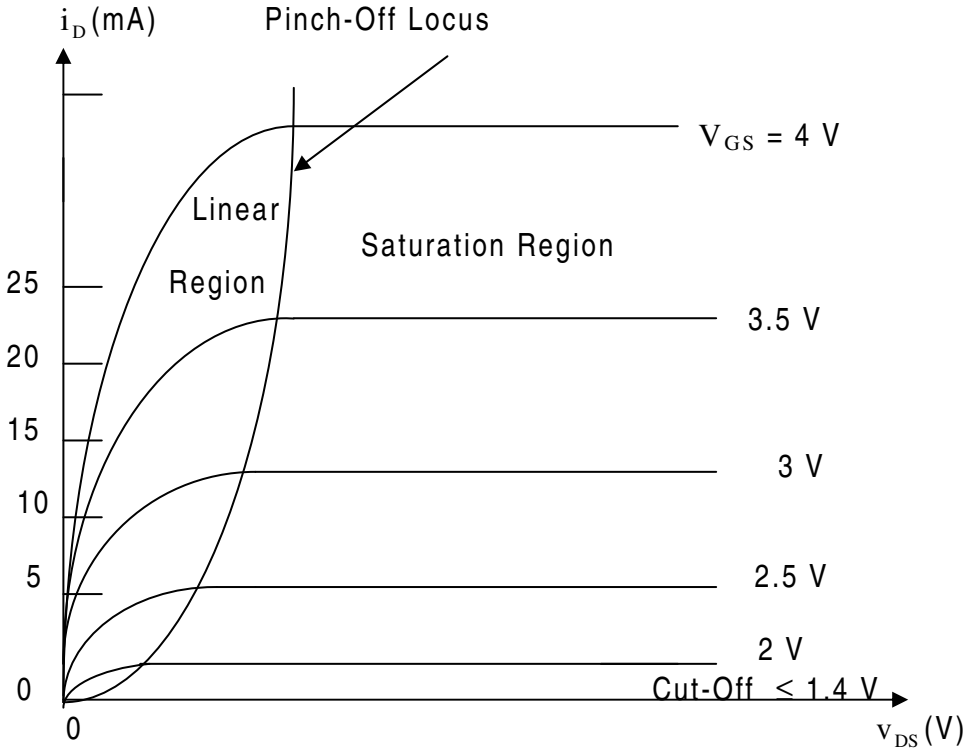


Figure 7.6: Drain current family of characteristics of an NMOS

A typical family of drain current characteristics is given in **Figure 7.6** for an NMOS. Note that the drain current is almost zero for $V_{GS} \leq V_T$ where V_T is about 1.4 V. Attempt has been made to reproduce the curves for NDS9410 as faithfully as possible with the limited graphing package. For this transistor, the drain current, at 25°C, has a maximum value of 2 μA when V_{GS} = 0 (zero-gate-voltage) and V_{DS} = 24 V. It becomes 25 μA when the case temperature rises to 125°C.

7.4 Schematic diagrams for an NMOS

The four-terminal schematic diagram for the n-channel MOSFET is given in **Figure 7.7a.** The solid line for the gate is separated by a broken line that shows the connections for the drain and the source. The space between the solid and the broken lines is for the channel and the broken line indicates its absence. In other words, the channel is yet to be induced. The arrow on the substrate points from the p-type substrate toward the n-channel that must be induced for the proper operation of the NMOS. The fabrication of the device creates an npn transistor (not shown) where the drain is the collector, the substrate is the base, and the source is the emitter.

In most applications, the source and the substrate are connected together. In fact, the manufacturer of the device may have already done it. The schematic for the three-terminal device is shown in **Figure 7.7b**. The npn transistor (not shown) now acts as a reverse biased diode when the drain is positive with respect to the source. This parasitic diode is a blessing in disguise when the transistor is used as a switch. A somewhat simplified symbol, **Figure 7.7c,** is also used where the broken line between the drain and the source further stresses the absence of the channel. The arrow now points in the direction of the current flow out of the source terminal. The current enters the device at the drain and exits at the source after passing through the channel.

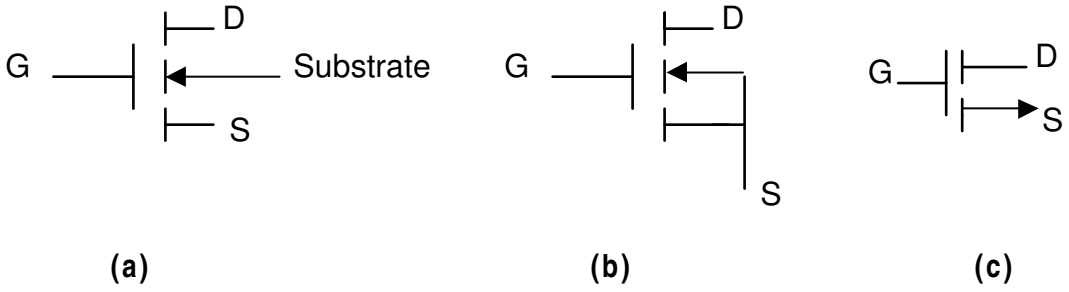


Figure 7.7: Various symbols for NMOS.

7.5 BIASING OF AN NMOS

Since an NMOS operates like any other transistor we have discussed so far, it can be biased using the same biasing schemes. The NMOS can only be turned ON by applying a positive voltage at the gate with respect to the source. The gate-to-source voltage must be greater than its threshold voltage. The DFET, on the other hand, has an advantage over the NMOS in the sense that it can be biased at the point where gate-to-source voltage is zero.

The NMOS enters the cut-off mode as soon as its gate-to-source voltage becomes equal or less than its threshold voltage. For an NMOS, the threshold voltage is greater than zero. For example, the typical value of the threshold voltage for NDS9410 is 1.4 V. As suggested by its manufacturer, National Semiconductor, it can vary from a minimum value of 1 V to a maximum value of 3 V. The key issue here is that the threshold voltage is greater than zero. In order to make the equations for the PMOS transistors (see next section) to look exactly like those for the NMOS transistor, we will us the absolute value of the threshold voltage.

7.6 EQUATIONS FOR AN NMOS

The appropriate equations for an NMOS are usually given in terms of the conduction parameter K_N. The conduction parameter depends upon the fabrication of an NMOS. It has been theoretically determined that K_N is a function of the length and width of the channel, the mobility of the major charge carriers in the channel, and thickness of the SiO_2 layer.

In the equation form, K_N is given as

$$K_N = \frac{1}{2}\mu_n C_{ox}\frac{W}{L} = \frac{k_n}{2}\frac{W}{L}$$

where μ_n is the electron mobility in the n-channel, W is the width and L is the length of the channel, and C_{ox} is the capacitance per unit area of the SiO_2 layer.

If ε_{ox} is the permittivity of the SiO_2 layer and t_{ox} is its thickness, then the capacitance per unit area of the SiO_2 layer is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (F/m^2)$$

The parameter $k_n = \mu_n C_{ox}$ is usually a constant quantity. Therefore, the conduction parameter K_N is directly proportional to the width and is inversely proportional to the length of the channel. The details of SiO_2 layer and the dimensions of the n-channel (below the layer) are shown in **Figure 7.8.**

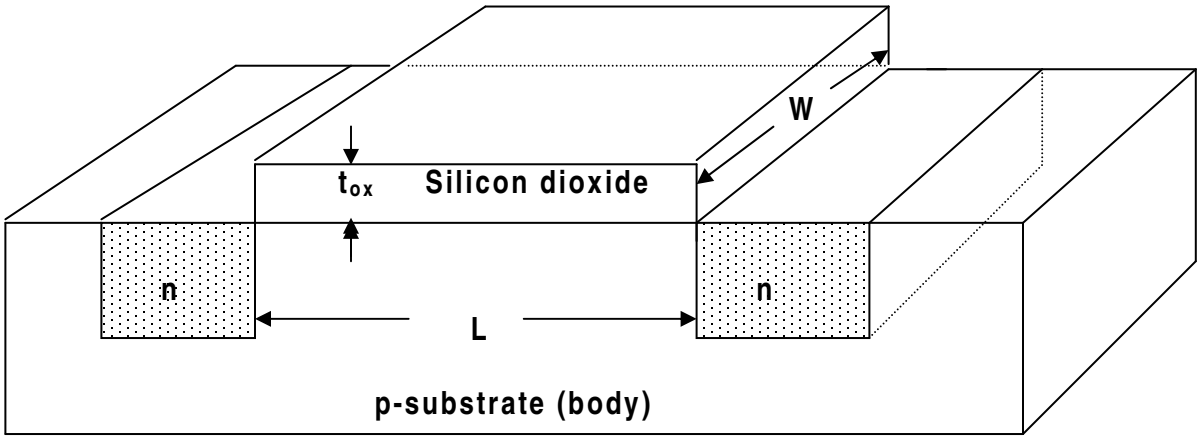


Figure 7.8: Details of SiO_2 layer

Equations for an NMOS

(a) Cut-off Region

$v_{GS} \le |V_T|$ where $V_T > 0$

$i_D = 0$

(b) Operation in the Saturation Region:

$$V_{DSP} = v_{GS} - |V_T|$$

Condition: $v_{DS} \ge V_{DSP}$

$$i_D = K_N (v_{GS} - |V_T|)^2$$

where $K_N = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} = k_n' \frac{W}{L}$

and $k_n' = \frac{1}{2} \mu_n C_{ox}$

Transconductance: For small-signal analysis.

$$g_m = 2 \sqrt{K_N I_{DQ}}$$

(c) Operation in the Linear (Triode or Ohmic) Region:

$$V_{DSP} = v_{GS} - |V_T|$$

Condition: $v_{DS} < V_{DSP}$

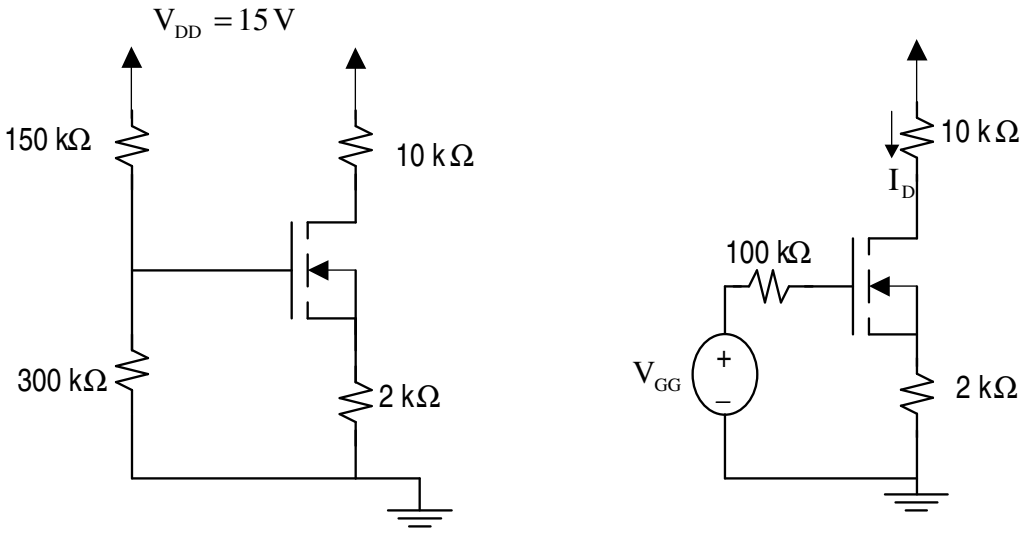
$$i_D = 2 K_N [v_{GS} - |V_T| - 0.5 v_{DS}] v_{DS}$$

where $K_N = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} = k_n' \frac{W}{L}$

and $k_n' = \frac{1}{2} \mu_n C_{ox}$

EXAMPLE 7.1: DC ANALYSIS OF AN NMOS TRANSISTOR _____

The NMOS transistor in **Figure 7.9a** has V_T = 1 V and K_N = 1 mA/V^2. Determine its region of operation.



(a) (b)

Figure 7.9: (a) The NMOS circuit, and (b) its dc equivalent circuit

DC Analysis

The biasing circuit can be replaced by its Thevenin equivalent circuit as shown in **Figure 7.9b** where

$$V_{GG} = 10\ V$$

$$R_G = 100\ k\Omega$$

(1) Can the transistor be in its cut-off mode?

When the transistor is in its cut off mode, the drain-to-source current I_D should be zero. Therefore, the source terminal is at 0 V. The gate current is zero. The gate terminal is at 10 V. Thus, the gate to source voltage, V_{GS} = 10 V. Since V_{GS} is greater than V_T, the device must be ON. **Hence, the NMOS is ON**.

(2) Is the NMOS operating in the saturation region?

To answer this question, let us assume that NMOS operates in the saturation (active) region. In this region, the drain current is almost constant as long as V_{DS} is greater than V_{DSP}.

In the following analysis, let us assume that all currents are in mA and all resistors are in kΩ. Then,

$$V_S = 2\ I_D$$

$$V_{GS} = V_G - V_S = 10 - 2\ I_D$$

The current in the NMOS, in the saturation region, is

$$I_D = K_N\ (V_{GS} - |V_T|)^2$$

$$= (1\ mA)\ (10 - 2\ I_D - 1)^2 = (9 - 2\ I_D)^2$$

The solution of this equation yields I_D = 5.693 mA or I_D = 3.557 mA. The drain current cannot be 5.693 mA because it forces the transistor to operate in its cut-off mode. Therefore, I_D = 3.557 mA. We can now compute other voltages as

$$V_S = 2\ I_D = 7.11\ V$$

$$V_{GS} = 10 - 2\ I_D = 2.89\ V$$

$$V_{DSP} = V_{GS} - |V_T| = 2.89 - 1 = 1.89\ V$$

$$V_{DS} = 15 - 12\ I_D = -\ 27.684\ V$$

Since V_{DS} cannot be negative, our assumption is wrong.

The NMOS must be operating in its linear (triode or ohmic) region.

(3) Does the transistor really operate in the linear region?

Let us now assume that the NMOS operates in the linear region. Then,

$$V_{GS} = 10 - 2\ I_D$$

$$V_{DS} = 15 - 12\ I_D$$

Using the current equation for the linear region, we have

$$I_D = 2\ K_N\ (V_{GS} - |V_T| - 0.5\ V_{DS})\ V_{DS}$$

Substituting the values, we obtain

$$I_D = (2\ mA)\{10 - 2\ I_D - 1 - 0.5(15 - 12\ I_D)\}\ (15 - 12\ I_D)$$

$$= 2\ (1.5 + 4\ I_D)(15 - 12\ I_D)$$

The solution of this equation yields

$$I_D = -\ 0.377\ mA \quad \text{or} \quad I_D = 1.242\ mA.$$

Since the drain current cannot be negative, it must be 1.242 mA.

For $I_D = 1.242$ mA,

$$V_{GS} = 10 - 2\ I_D = 7.516\ V$$

$$V_{DS} = 15 - 12\ I_D = 0.096\ V$$

$$V_{DSP} = V_{GS} - |V_T| = 7.516 - 1 = 6.516\ V$$

Since V_{DS} is less that V_{DSP}, the NMOS transistor does operate in its linear region. Thus, at the dc operating point (Q-point),

$$I_{DQ} = 1.242\ mA, \quad V_{DSQ} = 0.096\ V, \quad V_{GSQ} = 7.516\ V$$

In this region, the transistor behaves like an active resistor.

Let R_D be the active resistance of the transistor. Then

$$R_D = \frac{V_{DSQ}}{I_{DQ}} = \frac{0.096\ V}{1.242\ mA} = 77.3\ \Omega$$

EXAMPLE 7.2: _____

An NMOS transistor has K_N = 2 mA/V² and V_T = 0.5 V. It is used in the common-source (CS) configuration shown in **Figure 7.10**. Design the circuit so that its Q-point is at V_{DSQ} = 6 V and I_{DQ} = 8 mA, and R_{in} = 60 kΩ (± 5%). Select standard values of resistors. Determine the voltage, current, and power gains of the amplifier. If the peak-to-peak variation of the input voltage is 2 mV, what is the peak-to-peak variation of the output voltage?

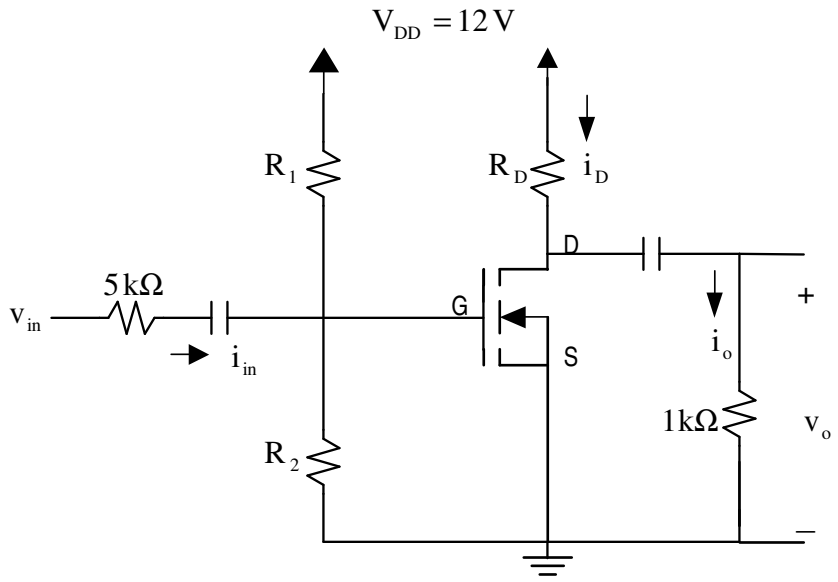


Figure 7.10: Common-source amplifier using an NMOS transistor

In the following analysis, all resistors are in kΩ and all currents are in mA.

For the transistor to act as an amplifier, it must operate in the saturation region. For I_{DQ} = 8 mA, the gate-to-source voltage V_{GSQ} can be computed from the following equation.

$$I_{DQ} = K_N (V_{GSQ} - |V_T|)^2$$

$$8 = 2 (V_{GSQ} - 0.5)^2$$

From this equation, we obtain V_{GSQ} = 2.5 V

The voltage at the transition point (separation of the linear region from the saturation region) is

$$V_{DSP} = V_{GSQ} - |V_T| = 2.5 - 0.5 = 2 \text{ V}$$

Since, the desired Q-point voltage V_{DSQ} (6 V) is greater than V_{DSP} (2V), the transistor operates in the saturation region.

For V_{DSQ} = 6 V, the voltage drop across R_D is 6 V. Thus

$$R_D = \frac{6 \text{ V}}{8 \text{ mA}} = 0.75 \text{ k}\Omega$$

Since a 750-Ω resistor is available with a ± 5% tolerance, we select

$$R_D = 750 \ \Omega.$$

For V_{GSQ} = 2.5 V and V_S = 0 V, V_G must be 2.5 V. Since I_G is zero, V_G must be V_{GG}. Thus, V_{GG} = 2.5 V. However,

$$V_{GG} = V_{DD} \frac{R_2}{R_1 + R_2}$$

$$2.5 = 12 \frac{R_2}{R_1 + R_2} \qquad (7.1)$$

The input resistance is equal to the parallel combination of R_1 and R_2. For the input resistance to be 60 kΩ, we have

$$60 = \frac{R_1 R_2}{R_1 + R_2} \qquad (7.2)$$

From (7.1) and (7.2): $\frac{2.5}{60} = \frac{12}{R_1}$

Thus, R_1 = 288 kΩ. We can use 220-kΩ resistor in series with a 68-kΩ resistor for R_1. It would be nice to use one resistor in order to reduce the inventory and manufacturing costs.

Form (7.1), we compute R_2 = 75.789 kΩ. Since R_2 requires more than two resistors in series, let us select a single resistor with a value of 75 kΩ for R_2. Using (7.1), we can now recompute R_1 as 285 kΩ. We can use 270-kΩ resistor in series with a 15-kΩ resistor for R_1.

Using (7.1) to recompute R_1 ensures that V_{GSQ} will still be 2.5 V.

However, the input resistance would now be

$$R_{in} = (75\ k\Omega)//(285\ k\Omega) = 59.375\ k\Omega$$

Since we are allowed to have ±5% variations in the input resistance, the lowest acceptable value of the input resistance is 57 kΩ (0.95 × 60 kΩ). Since R_{in} is greater than 57 kΩ, it satisfies the design requirements.

Thus, we will use the following values of resistors:

$R_D = 750\ \Omega$

$R_2 = 75\ k\Omega$

and $R_1 = 285\ k\Omega$ (A 270-kΩ resistor in series with a 15-kΩ resistor)

The dc Load line

The equation for the dc load line is

$$12 = 0.75\ I_D + V_{DS}$$

The two points on the dc load line can be computed as follows:

(a) When $I_D = 0$, the dc voltage drop across the transistor is maximum. Let us denote it as V_{DCM}. Thus, when $I_D \rightarrow 0$, $V_{DS} \rightarrow V_{DCM} = 12$ V.

(b) When the voltage drop across the transistor is zero, then the current in the transistor is at its maximum. Let us denote the maximum current as I_{DCM}. Thus, when $V_{DS} \rightarrow 0$, $I_D \rightarrow I_{DCM} = 16$ mA.

The dc load line can now be plotted as shown in **Figure 7.11**.

AC Analysis:

Let us now compute the transconductance for the ac analysis using the equation

$$g_m = 2\sqrt{K_N\ I_{DQ}} = 2\sqrt{2 \times 8} = 8\ \text{mS}$$

The small-signal ac equivalent circuit of the NMOS is given in **Figure 7.12**.

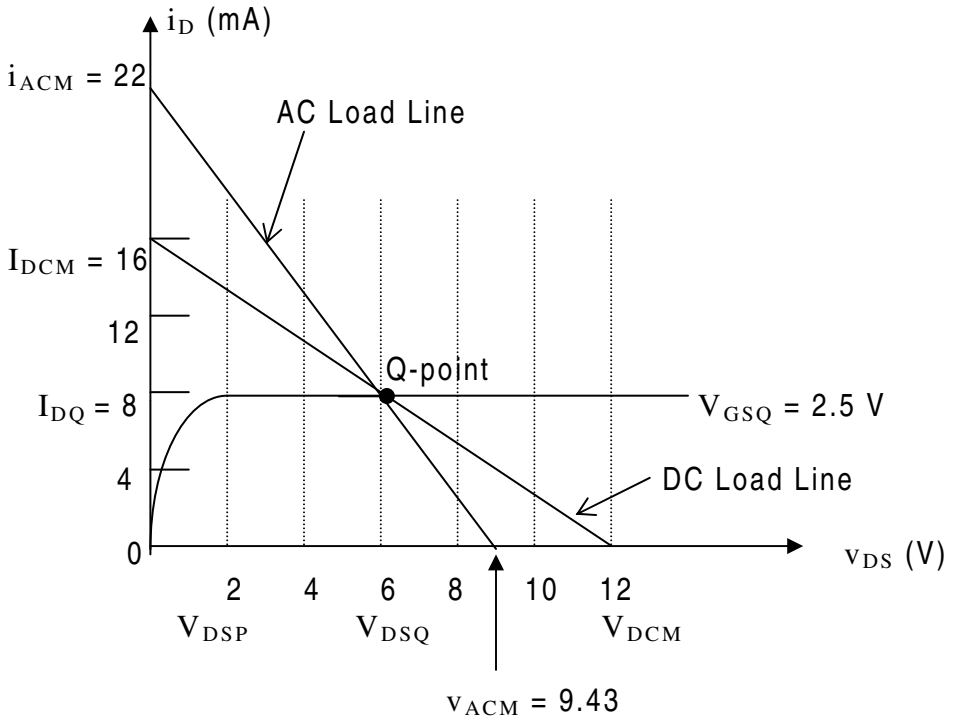


Figure 7.11: DC and ac load lines

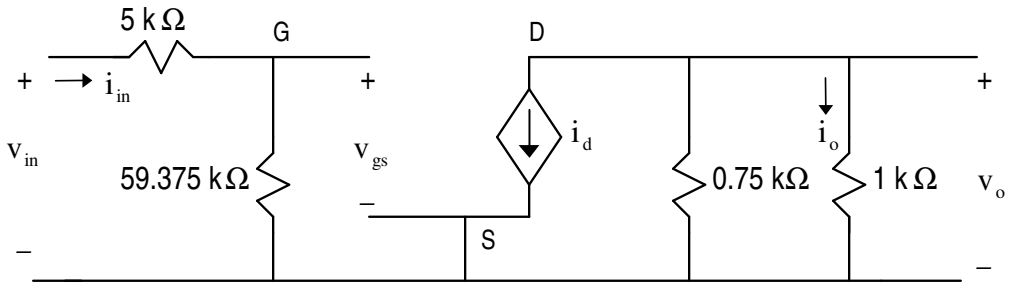


Figure 7.12: Small-signal circuit

$$v_{gs} = \frac{59.375}{59.375 + 5} v_{in} = 0.922\, v_{in}$$

$$i_d = g_m v_{gs} = (8\ \text{mS})\ (0.922\ v_{in}) = 7.376\ v_{in} \quad (\text{mA})$$

The output current: $i_o = -\frac{0.75}{1.75}(7.376\, v_{in}) = -3.16\, v_{in}$ (mA)

The output voltage: $v_o = i_o R_L = -\ 3.16\ v_{in}$ (V)

Hence, the overall voltage gain: $A_V = -\ 3.16$

The input current: $i_{in} = \frac{v_{in}}{64.375}$ (mA)

Hence, the current gain: $A_I = -\ 203.425$

Finally, the power gain: $A_P = A_V A_I = 642.823$

AC Load line:

We are now in a position to draw the ac load line as illustrated in **Figure 7.11**. The ac load line passes through the Q-point. It intersects the voltage axis at v_{ACM} such that

$$v_{acM} = V_{DSQ} + I_{DQ} R_{AC}$$

The ac resistance: $R_{AC} = (0.75\ \text{k}\Omega)//(1\ \text{k}\Omega) = 0.4286\ \text{k}\Omega$.

Substituting in the above equation, we get $v_{ACM} = 9.43$ V

The ac load line intersects the current axis at

$$i_{ACM} = \frac{9.43\ \text{V}}{0.4286\ \text{k}\Omega} = 22\ \text{mA}$$

When the input signal has a peak-to-peak variation of 2 mV, the output signal will have a peak-to-peak variation of 6.32 mV ($A_V v_{in}$). The amplified output signal, however, is 180° out of phase with respect to the input signal.

7.7 PROBLEMS: NMOS

7.1 An NMOS **common-source** amplifier circuit is given in **Figure P7.1** where R_D = 4 kΩ, R_S = 2 kΩ, R_L = 6 kΩ, R_1 = 200 kΩ, and R_2 = 100 kΩ. The transistor parameters are K_N = 0.5 mA/V², and V_T = 2 V. Determine the dc operating point and sketch the dc and ac load lines. Calculate the small-signal voltage, current, and power gains. What are the input and output resistances?

7.2 If the source resistance R_S is bypassed by a large capacitor and the load resistance R_L is removed from the circuit in **Figure P7.1**, determine the voltage, current, and power gains for the modified circuit. What are the input and output resistances in this case?

7.3 Repeat **Problem 7.1** if the input signal has an internal resistance of 5 kΩ.

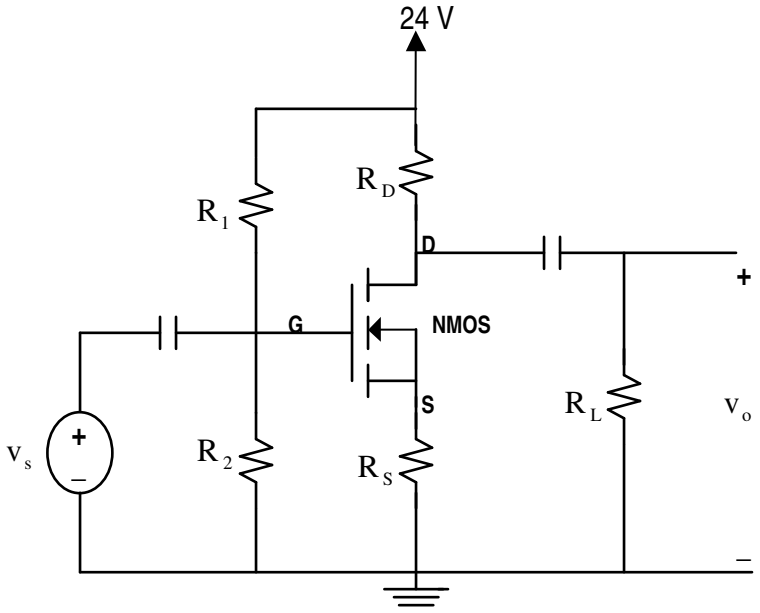


Figure P7.1

7.4 An NMOS **common-drain** amplifier circuit is given in **Figure P7.4** where R_1 = 100 kΩ, R_2 = 200 kΩ, R_S = 2 kΩ, and R_L = 0.5 kΩ. The parameters of the transistor are K_N = 0.75 mA/V² and V_T = 2 V. Determine the dc operating point and sketch the dc and ac load lines. Calculate the small-signal voltage, current, and power gains. What are the input and output resistances?

7.5 If the load resistance R_L is removed from the circuit in **Figure P7.4**, determine the voltage, current, and power gains for the modified circuit. What are the input and output resistances in this case?

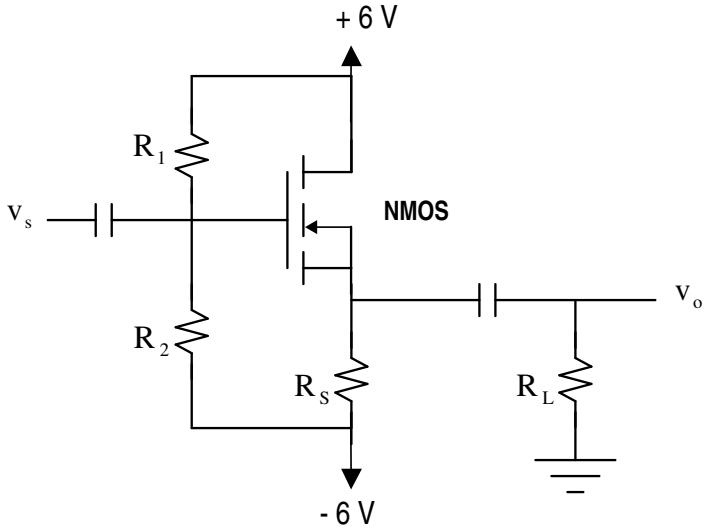


Figure P7.4

7.6 The parameters of the NMOS transistor in the **common-gate** amplifier circuit of **Figure P7.6** are K_N = 1.2 mA/V² and V_T = 1.4 V. The resistors in the circuit are R_1 = 60 kΩ, R_2 = 40 kΩ, R_S = 2 kΩ, R_D = 3 kΩ, and R_L= 3 kΩ. Determine the dc operating point and sketch the dc and ac load lines. Calculate the small-signal voltage, current, and power gains. What are the input and output resistances?

7.7 If the load resistance R_L is removed from the circuit in **Figure P7.6**, determine the voltage, current, and power gains for the modified circuit. What are the input and output resistances in this case?

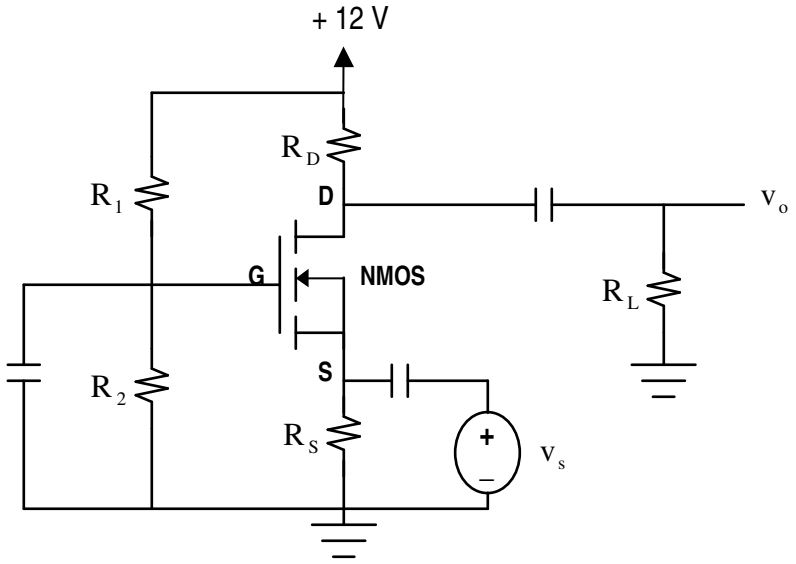


Figure P7.6